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DOCUMENT-IDENTIFIER: US 6345310 B1
TITLE: Architecture for a multiple port adapter having a single media access control (MAC) with a single I/O port

Abstract Text (1):
A multiple port adapter having a single MAC chip with a single I/O port has reduced logic circuits and I/O pins for transferring data between a host system and a TDM communication system. The MAC chip includes a transmit MAC and a receive MAC, each coupled at one end through the single I/O port to a port multiplexer and at the other end to respective storage registers. The port multiplexer is coupled to each port. Transmit and receive state registers track the state of each port in the transfer of data in the transmit and receive directions through the single I/O port. The storage registers are coupled through a host bus interface to a host bus and to the host system. Control logic is coupled to the storage register to control the transfer of data between the system and the storage registers. A port selector coupled between the multiplexer and the transmit and receive state registers selects ports for transfer of data in succession. On each chip clock cycle, the port selector selects a state machine register to determine the state of the MACs for processing the data and a section of the FIFO's to write or read data for the selected port. At the end of the cycle, the state registers are set and stay set until selected again. The process repeats for each port in a cyclic manner. Once data is accumulated in the receive storage register, control logic reads the data of the host bus. Once space is available in the transmit storage register, the control logic writes data from the host system to the transmit storage register.

Brief Summary Text (22):
These and other objects, features and advantages are achieved in a single MAC coupled between a host system and a time division, multi-channel network. The single MAC has a single I/O port and includes a transmit MAC and a receive MAC path. Each path is coupled at one end to the I/O pins and at the other end to separate transmit and receive storage (FIFO) devices. A transmit state machine is coupled to the transmit MAC and transmit FIFO. A receive state machine is coupled to the receive MAC and receive FIFO. Each FIFO is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network. A port selector is coupled to the multiplexer and to the transmit and receive state machines for selecting each port on a cyclic basis to transmit and receive data. Each state machine contains a state table having a one word entry for each port to track the status of the port. The I/O pins are coupled to a Physical Layer containing a multiplexer connected to each port serving a channel in the network through a Media Independent register. As the ports are selected by the port selector, the associated word for a port is read from the table and used to control the state machine in servicing the port. The port selector also assigns a section in the FIFO's for storing data processed or to be processed by the MACs. The transmit and receive state machines operate concurrently and determine the MAC state for servicing the port, after which the MAC state is updated and stored back into the state table. In the receive direction, the ports are serviced in a round robin fashion. In the transmit direction, data is written into the transmit FIFO as space becomes available. Control Logic means controls the transfer of data between the host system and the network and vice-a-versa when instructed by the FIFOs. The chip architecture is extendable from 10 mbps to 100 mbps and reduces the I/O pin count for the adapter and the MAC chip logic by approximately 75% compared to prior art devices.

CLAIMS:

4. The multiple port adapter of claim 3 further comprising control logic and a host interface and wherein the storage device provides instructions to the control logic for transmitting and receiving data between the host system and the network.

17. The system of claim 14 wherein the storage device are coupled to a host interface and provides instructions to the control logic for transmitting and receiving data through the single I/O port between the host system and the network.

20. In a communication network coupled to a multiple port adapter, a Media Access Control (MAC) coupled to through single I/O port to a multiplexer for servicing multiple adapter ports on an individual basis, interface means coupled through the single I/O port to the multiplexer and the MAC, a state machine for tracking the transfer of data between a host system and the network, storage means coupled to the host system and the MAC and control logic for transferring data to and from the host system and the storage means, a port selector selecting individual ports on a cycle basis coupled to the multilexer and the state machine, a method for connecting the MAC to each port on an individual basis for the transfer of data, in both directions, through the single I/O port between the host system and the network, comprising the steps of:

a) selecting a port to transfer data between the host system and the network through the single I/O port using the port selector;

b) connecting the selected port to the multiplexer and the interface means in a clock cycle;

c) transmitting a preamble and start frame delimiter in a transmit frame; calculating the frame CRC and signalling any errors in the frame to a physical layer serving the selected port using the interface means;

d) stripping the preamble and start frame delimiter in a received frame; calculating and checking the CRC of the frame, and passing the destination address, source address, type/length field, frame payload to the MAC through the single I/O port using the interface means;

e) selecting the state registers for the selected port using the state machine as instructed by the port selector;

f) selecting the section of the storage device to move data out of or store data in using the port selector;

g) processing data in the MAC device provided by the interface means or the storage means and writing data in and/or reading data out of the storage means;

h) updating the state machine on an individual port basis with regard to the data transferred to the network and to the storage device;

i) providing instruction to the control logic for transferring data to/from the storage device and the host system; and

j) repeating steps a)-h) for the next clock cycle.